What is claimed is:

1. A device, comprising:

a layer of a first conductivity type;

a first transistor disposed in the layer;

a body contact region disposed in the layer; and

a resistance region disposed in the layer between the first transistor and the body contact region, the resistance region having a resistivity higher than a resistivity of the layer.

2. The device of claim 1, further comprising:

a second transistor disposed in the layer, wherein the second transistor is disposed on a same side of the resistance region as the body contact region.

3. The device of claim 1, wherein the body contact region is adapted to be coupled to ground and the first conductivity type is p-type.

4. The device of claim 1, wherein the body contact region is adapted to be coupled to a power supply voltage and the first conductivity type is n-type.

5. The device of claim 1, further comprising a substrate, the layer being disposed on top of the substrate.

6. The device of claim 1, wherein the resistance region has an impurity concentration lower than an impurity concentration of the layer.

7. The device of claim 1, further comprising a discrete capacitor coupled between a body and a source of the first transistor.

8. The device of claim 1, wherein the resistance region occupies substantially an entire cross-sectional area of the layer between the first transistor and the body contact region.

9. The device of claim 1, further comprising:

a second transistor coupled in series with the first transistor and having a control electrode adapted to receive an input signal of the device, the first transistor having a control electrode adapted to receive a bias voltage, and the body contact region being adapted to be coupled to a first one of a power supply voltage and ground; and

a load having a first end coupled to the first transistor and a second end adapted to be coupled to a second one of the power supply voltage and ground, a body of the second transistor being adapted to be coupled to the first one of the power supply voltage and ground.

10. The device of claim 9, wherein the first and second transistors are n-type conductivity transistors.

11. The device of claim 9, wherein the resistance region is adapted to substantially isolate a body of the first transistor from ground.

12. The device of claim 9, wherein the resistance region is adapted to substantially isolate a body of the first transistor from ground when the input signal is at or above a predetermined operating frequency.

13. The device of claim 9, wherein the load is an inductance.

14. The device of claim 1, wherein the layer is an epitaxial layer.

15. A system, comprising:

a signal generating device;

an amplifying device adapted to receive an input signal from the signal generating device and adapted to output an output signal, the amplifying device comprising:

a first transistor having a control electrode adapted to receive a bias signal and a body adapted to be coupled to a first one of a power supply voltage and ground through a resistance, wherein the resistance is high enough to substantially isolate the body of the first transistor from the first one of the power supply voltage and ground;

a second transistor coupled in series to the first transistor and having a control electrode adapted to receive the input signal; and

a load having a first end coupled to the first transistor and a second end adapted to be coupled to a second one of the power supply voltage and ground, the first end being adapted to output the output signal; and

an output device coupled to the amplifying device and adapted to receive the output signal from the amplifying device.

16. The system of claim 15, wherein the signal generating device produces an RF input signal as the input signal.

17. The system of claim 15, wherein the first transistor is disposed in a layer, the layer comprising:

a body contact region disposed in the layer; and

a resistance region disposed in the layer between the first transistor and the body contact region, the resistance region having a resistivity higher than a resistivity of the layer.

18. The system of claim 17, wherein the second transistor is disposed in the layer, and wherein the second transistor is disposed on the same side of the resistance region as the body contact region.

19. The system of claim 15, wherein the first and second transistors are n-type conductivity transistors.

20. The system of claim 15, wherein the load comprises an antenna.

21. The system of claim 15, wherein the load comprises an omnidirectional antenna.

22. A method, comprising:

producing a substrate and a layer on top of the substrate;

masking a resistance region of the layer between a first transistor region and a second transistor region;

implanting the layer with impurities to lower a resistivity of the first transistor region and the second transistor region; and

forming a first transistor in said first transistor region, wherein a resistivity of the resistance region is sufficiently high to substantially isolate the first transistor region from the second transistor region when an input signal applied to the first transistor is at or above a predetermined frequency.

23. The method of claim 22, further comprising forming a body contact region in the second transistor region, and wherein the resistance region is formed between the first transistor region and the body contact region.

24. The method of claim 23, further comprising:

forming a second transistor in the second transistor region.